

REMARKS

The Office action of September 10, 2008, has been carefully considered.

The specification has been amended to add a reference to the originally filed PCT application, and to add proper subject matter headings.

Claims 4-5 have been objected to, and the objections have been obviated by the claims as rewritten.

Claims 1, 16 and 19-22 have been rejected under 35 USC 103(a) over Dory in view of Fairley et al.

Claims 1-22 have now been canceled and rewritten as a new set of Claims 23-44, written in proper form for U.S. practice. The invention is directed to a method for processing signals generated during the non-destructive examination of objects, for example pipes or sheet metal, by reflection of ultrasonic waves at defect locations of the structure of the object. According to the invention, a complete wave front is emitted onto at least one section of the object to be examined by means of a plurality of independent transmitter elements, a wave reflected by the structure of the object is received by a plurality of receiver elements which are independent of one another, the signals received are digitalized and the digitalized signals are stored according to amplitude and propagation time in a storage element. The invention is further directed to a circuit arrangement for processing signals generated during non-destructive examination of objects, comprising a single recording unit with a pulse generator for actuating transmitter/receiver elements for emitting a complete wave front and for switching the transmitter/received elements to receive, with a multiplexer provided by which analog signals applied to receiver elements can be transmitted to analog/digital converters, the outputs

of which are connected to a storage element for storing digitalized signals.

According to the improvement of the invention, defect locations are detected by the addition of stored amplitude values along a propagation time, which is referred to as a *phase-locked addition*. The apparatus for carrying out this process includes the storage element which stores the digitalized signals with respect to amplitude and propagation time, and a summing element for the phase-locked addition of the amplitude values stored in the storage element, which is arranged tandem behind the storage element. A signal which can be evaluated with respect to the defect location is applied to the output of the summing circuit.

The Office action alleges that Dory discloses a method for processing signals generated during non-destructive examination of objects by emitting a complete wave front onto at least one section of the object to be examined by a plurality of independent transmitter elements, and reception of the wave reflected by the structure of the object by means of a plurality receiver elements. The signals received are then digitalized.

The Office action states that while the data of the stored digitalized signals can be processed by logic circuits enabling identification and recording of the type of faults detected, it does not disclose that the defect locations are detected by a phase-locked addition of the stored amplitude values along the propagation time. However, the Office action then alleges that "Fairley discloses a phase-locked loop 10 at the summing unit 34 which summed the amplitude of the voltage of the square wave dithering signal (col. 5, lines 33-37). The summing circuit 60 sums the output from resistor 56 without from a phase detector (multiplier) 70 in the

phase-locked loop 52. It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize in Dory the phase locked loop of Fairley because it would include a dithering signal to the clock signal in the measuring device to change the time at which the phases of the two measured signals are compared and then averages the results over a period of the dithering signal to obtain the phase difference..."

Fairley et al, however, does not disclose the process of the invention. Fairley et al relates to a phase measurement system using a dithered clock, a technical field unrelated to the invention. The phase measurement system described in Fairley et al measures the phase shift between two signals by dithering a clock signal and averaging a plurality of measurements of the phase differences between the two signals. See column 1, lines 58-63. In Fairley et al, the phase-locked loop is one in which the frequency of the reference input signal is multiplied up to 8 times to generate a height frequency, and a dithering signal is added to the clock signal in the phase-locked loop to produce a dithered clock signal, in which a summing unit is added to a conventional phase-locked loop.

This is not the process of the invention, which makes no use of a reference signal or of a phase-locked loop.

According to the invention, the stored amplitude values of the signals received at the same propagation time, e.g. FE2 and FE5; FE3, FE6, and FE9; or FE4, FE7 and FE10, are added along the propagation time, as shown in Figures 2 and 5. The term "phase-locked addition" is unrelated to the phase-locked loop described in Fairley et al, since "phase-locked addition" expresses, according to Applicants' definition, that stored amplitude values with the same propagation time are added to each other.

There is absolutely no suggestion in Fairley et al of adding together stored amplitude values with the same propagation time.

Withdrawal of this rejection is requested.

Claims 2-6 and 17-18 have been rejected under 35 USC 103(a) over Dory in view of Thornell and Schmitz, Claim 7 has been rejected under 35 USC 103(a) over Dory in view of Thornell and further in view of Phelan, and Claim 8 has been rejected under 35 USC 103(a) over Dory in view of Thornell and Benedetto et al.

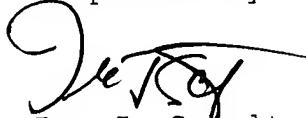
Applicant notes that these rejections do not cite the Fairley et al reference cited against claim 1, and do not explain the relevance of the Thornell reference. Hence, Applicants cannot argue against the citation of Thornell.

Regardless, Schmitz, Phelan and Benedetto et al do not cure the defects of the Dory and Fairley et al references, and withdrawal of these rejections is requested.

The allowability of Claims 9-15 has been noted.

In view of the foregoing amendments and remarks, Applicants submit that the present application is now in condition for allowance. An early allowance of the application with amended claims is earnestly solicited.

Respectfully submitted,



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